THE INVENTION CLAIMED IS:

1. A method of manufacturing an integrated circuit comprising;

providing a substrate having a semiconductor device thereon;

forming a first stop layer over the substrate;

forming a first dielectric layer over the first stop layer;

forming an opening having sidewalls in the first dielectric layer;

forming a first conformal barrier liner in the opening;

processing the first conformal barrier liner to remove horizontal portions and leave vertical portions of the first conformal barrier liner on the sidewalls of the opening in the first dielectric layer, the processing the first conformal barrier liner including removing a portion of the first stop layer to the semiconductor device;

treating the first conformal barrier liner and the first stop layer to increase adhesion properties thereof; and

forming a first conductor core in the opening over the vertical portions of the first conformal barrier liner and the first stop layer, forming the first conductor core includes connecting the first conductor core to the semiconductor device.

2. The method of manufacturing an integrated circuit as claimed in claim 1 including:

forming a via stop layer over the first dielectric layer;

forming a via dielectric layer over the via stop layer;

forming a second stop layer over the via dielectric layer;

forming a second dielectric layer over the via dielectric layer;

forming an opening having sidewalls in the second dielectric layer, through the via stop layer, and in the via dielectric layer;

forming a second conformal barrier liner in the opening;

processing the second conformal barrier liner to remove horizontal portions and leave vertical portions of the second conformal barrier liner on the sidewalls of the opening in the second dielectric layer and the via dielectric layer, the portions of the second conformal barrier liner on the sidewalls acting as a barrier to diffusion of conductor core material to the second dielectric layer and the via

dielectric layer, processing the second conformal barrier liner including removing a portion of the via stop layer to the first conductor core;

treating the second conformal barrier liner and the second stop layer to increase adhesion properties thereof; and

forming a second conductor core in the opening over the vertical portions of the second conformal barrier liner, the first conductor core, and the second stop layer, forming the second conductor core includes connecting the second conductor core to the first conductor core.

3. The method of manufacturing as claimed in claim 2 wherein forming the second stop layer forms a second stop layer having at least about twice the thickness of the first stop layer.

4. The method of manufacturing as claimed in claim 1 wherein treating the first conformal barrier liner uses a treatment selected from a group consisting of pre-cleaning, silicon-enrichment, wetting layer deposition, and a combination thereof.

5. The method of manufacturing as claimed in claim 1 wherein the first conductor core is a material selected from a group consisting of copper, aluminum, gold, silver, compounds thereof, and combinations thereof.

6. The method of manufacturing as claimed in claim 1 wherein forming the first dielectric layer deposits a low dielectric constant material.

7. An integrated circuit comprising;

a substrate having a semiconductor device thereon;

a first stop layer over the substrate having a portion open to the semiconductor device;

a first dielectric layer over the first stop layer having an opening provided therein having sidewalls in the first dielectric layer;

a first conformal barrier liner in the opening, the first conformal barrier liner having only vertical portions on the sidewalls of the opening in the first dielectric layer, the vertical portions of the first conformal barrier liner on the sidewalls acting as a barrier to diffusion of conductor core material to the first dielectric layer;

a treated area on the first conformal barrier liner and the first stop layer to increase adhesion properties thereof; and

a first conductor core in the opening over the vertical portions of the first conformal barrier liner and the first stop layer, the first conductor core connected to the semiconductor device.

8. The integrated circuit as claimed in claim 7 including:

a via stop layer over the first dielectric layer and having an opening provided therein;

a via dielectric layer over the via stop layer and having a via opening provided therein having sidewalls;

a second stop layer over the via dielectric layer and having an opening provided therein;

a second dielectric layer over the via dielectric layer having a channel opening provided therein having sidewalls;

a second conformal barrier liner in the opening, the second conformal barrier liner having only vertical portions on the sidewalls of the openings in the second dielectric layer and the via dielectric layer;

a treated area on the second conformal barrier liner and the second stop layer for increasing adhesion properties thereof; and

a second conductor core in the opening over the vertical portions of the second conformal barrier liner, the first conductor core, and the second stop layer, the second conductor core connected to the first conductor core through the opening in the via stop layer.

9. The integrated circuit as claimed in claim 8 wherein the first stop layer over the substrate has a thickness "t" and the via stop layer has a thickness "T" of greater than about 2t.

10. The integrated circuit as claimed in claim 7 wherein the first conformal barrier liner has a region selected from a group consisting of silicon-enriched, wetting layer covered, and a combination thereof.

11. The integrated circuit as claimed in claim 7 wherein the first conformal barrier liner is a nonconductive barrier material selected from a group consisting of a nitride, a BLok, a carbide, an oxynitride, and a combination thereof.

12. The integrated circuit as claimed in claim 7 wherein the first conductor core is a material selected from a group consisting of copper, aluminum, gold, silver, compounds thereof, and combinations thereof.

13. The integrated circuit as claimed in claim 7 wherein the first dielectric layer, the via dielectric layer, and the second dielectric layer are of low dielectric constant materials.

14. An integrated circuit comprising;

a substrate having a semiconductor device thereon;

a device dielectric layer over the substrate;

a first channel stop layer over the substrate and the device dielectric layer having a portion open to the semiconductor device;

a first channel dielectric layer over the first channel stop layer having a first channel opening provided therein having sidewalls in the first channel dielectric layer;

a first conformal barrier liner in the opening, the first conformal barrier liner having only vertical portions on the sidewalls of the opening in the first channel dielectric layer, the vertical portions of the first conformal barrier liner on the sidewalls acting as a barrier to diffusion of conductor core material to the first channel dielectric layer;

a treated area on the first conformal barrier liner and the first channel stop layer to increase adhesion properties thereof; and

a first conductor core in the opening over the vertical portions of the first conformal barrier liner and the first channel stop layer, the first conductor core connected to the semiconductor device.

15. The integrated circuit as claimed in claim 14 including:

a via stop layer over the first channel dielectric layer and having an opening provided therein;

a via dielectric layer over the via stop layer and having a via opening provided therein having sidewalls;

a second channel stop layer over the via dielectric layer and having a stepped opening provided therein, a first portion of the stepped opening of the same size as the opening in the first channel dielectric layer and a second portion of the stepped opening of the same size as the opening in the via stop layer;

a second channel dielectric layer over the via dielectric layer having a second channel opening provided therein having sidewalls;

a second conformal barrier liner in the opening, the second conformal barrier liner having only vertical portions on the sidewalls of the second channel opening

and the via opening in the second channel dielectric layer and the via dielectric layer, the vertical portions of the second conformal barrier liner on the sidewalls acting as a barrier to diffusion of conductor core material to the second channel dielectric layer and the via dielectric layer;

a treated area on the second conformal barrier liner and the second stop layer to increase adhesion properties thereof; and

a second conductor core in the opening over the vertical portions of the second conformal barrier liner, the first conductor core, and the second stop layer, the second conductor core connected to the first conductor core through the opening in the via stop layer.

16. The integrated circuit as claimed in claim 15 wherein the via stop layer over the substrate has a thickness "t" and the second channel stop layer has a thickness "T" of greater than about twice the thickness "t" distal from the stepped opening.

17. The integrated circuit as claimed in claim 14 wherein the first and second conformal barrier liners have regions selected from a group consisting of silicon-enriched, wetting layer covered, and a combination thereof.

18. The integrated circuit as claimed in claim 14 wherein the first conformal barrier liner and the second conformal barrier liner are nonconductive barrier materials selected from a group consisting of a nitride, a BLok, a carbide, an oxynitride, and a combination thereof in a thickness between 20 Å and 70Å.

19. The integrated circuit as claimed in claim 14 wherein the first channel dielectric layer, the via dielectric layer, and the second channel dielectric layer are of porous low dielectric constant materials having dielectric constants under 3.9.

20. The integrated circuit as claimed in claim 14 wherein the first conductor core and the second conductor core are materials selected from a group consisting of copper, aluminum, gold, silver, compounds thereof, and combinations thereof.